SDAS228A - JUNE 1982 - REVISED JANUARY 1995

- Compare Two 8-Bit Words
- Totem-Pole Outputs $(\overline{P} = \overline{Q})$
- 'ALS688 Are Identical to 'ALS521
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

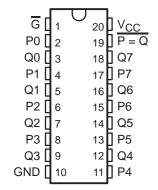
These identity comparators perform comparisons on two 8-bit binary or BCD words and provide $\overline{P} = \overline{Q}$ outputs. These devices have totem-pole outputs.

The SN54ALS688 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74ALS688 is characterized for operation from 0°C to 70°C.

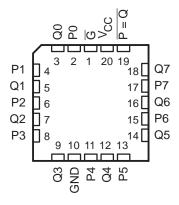
FUNCTION TABLE

IN	PUTS	OUTDUT
DATA P, Q	ENABLE G	OUTPUT P = Q
P = Q	L	L
P > Q	L	Н
P < Q	L	Н
X	Н	Н

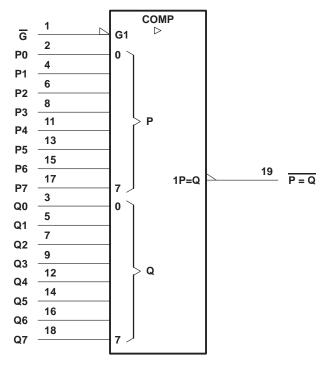
SN54ALS688 . . . J PACKAGE SN74ALS688 . . . DW OR N PACKAGE (TOP VIEW)



SN54ALS688 . . . FK PACKAGE (TOP VIEW)



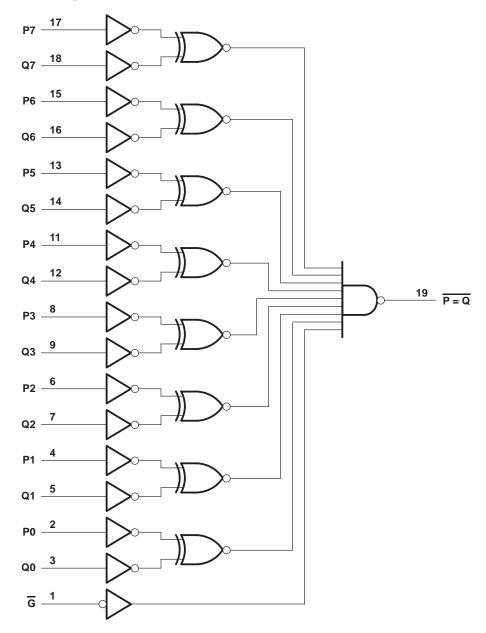
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{CC}	7 V
Input voltage, V _I	7 V
Operating free-air temperature range, T _A : SN54ALS688	–55°C to 125°C
SN74ALS688	0°C to 70°C
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



SN54ALS688, SN74ALS688 **8-BIT IDENTITY COMPARATORS**

SDAS228A - JUNE 1982 - REVISED JANUARY 1995

recommended operating conditions

		SN54ALS688			SN	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vсс	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
loh	High-level output current			-1			-2.6	mA
loL	Low-level output current			12			24	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST OF	SN	54ALS6	88	SN	LIAUT			
PARAMETER	IEST CC	ONDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	V _{CC} = 4.5 V,	$I_{I} = -18 \text{ mA}$			-1.5			-1.5	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2	2		V _{CC} -2	2		
Voн	V _{CC} = 4.5 V	$I_{OH} = -1 \text{ mA}$	2.4	3.3					V
	VCC = 4.5 V	$I_{OH} = -2.6 \text{ mA}$				2.4	3.3		
VOL	V _{CC} = 4.5 V	$I_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4	V
VOL.	VCC = 4.5 V	$I_{OL} = 24 \text{ mA}$					0.35	0.5	V
lį	$V_{CC} = 5.5 \text{ V},$	V _I = 7 V			0.1			0.1	mA
lН	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μΑ
I _{IL}	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.1			-0.1	mA
I _O ‡	V _{CC} = 5.5 V,	V _O = 2.25 V	-20		-112	-30		-112	mA
Icc	$V_{CC} = 5.5 \text{ V},$	See Note 1		12	19		12	19	mA

switching characteristics (see Figure 1)

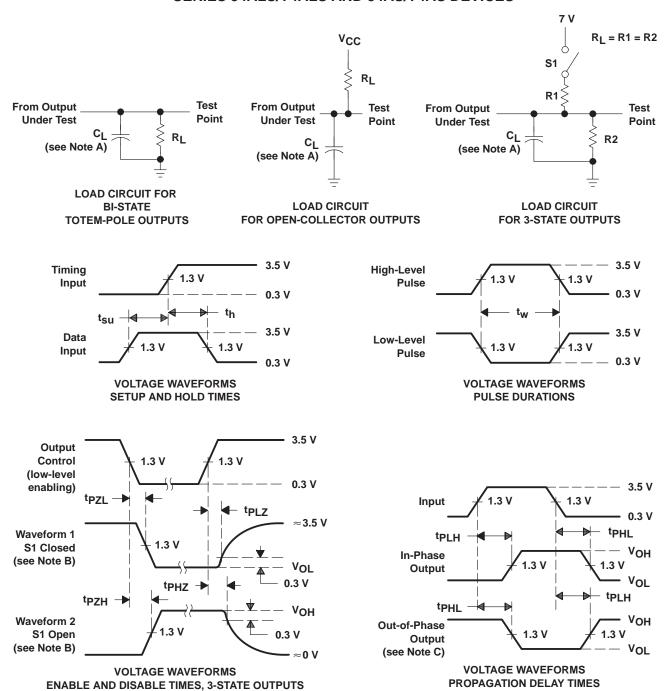
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _C C _L R _L T _A	UNIT			
			SN54A	LS688	SN74A		
			MIN	MAX	MIN	MAX	
^t PLH	Р	$\overline{P} = Q$	3	16	3	12	ns
^t PHL	P	P=Q	5	25	5	20	115
^t PLH	0	$\overline{P} = Q$	3	16	3	12	20
^t PHL	Q	P = Q	5	25	5	20	ns
t _{PLH}	G	$\overline{P} = Q$	3	15	3	12	ns
t _{PHL}	G	Γ≡Q	5	25	5	22	115

[§] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



[†] All typical values are at $V_{CC} = 5$ V, $T_A = 25^{\circ}$ C. ‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{CC} . NOTE 1: I_{CC} is measured with \overline{G} grounded, P and Q at 4.5 V.

PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- D. All input pulses have the following characteristics: PRR \leq 1 MHz, t_{Γ} = t_{f} = 2 ns, duty cycle = 50%.
- E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms









PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-88578012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8857801RA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
5962-8857801SA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
SN54ALS688J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SN74ALS688DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS688DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS688DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS688DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS688DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS688DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS688N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS688N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74ALS688NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS688NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS688NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS688NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54ALS688FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54ALS688J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54ALS688W	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



PACKAGE OPTION ADDENDUM

18-Sep-2008

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS688DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74ALS688NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS688DWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74ALS688NSR	SO	NS	20	2000	346.0	346.0	41.0

MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004



14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20



DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



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